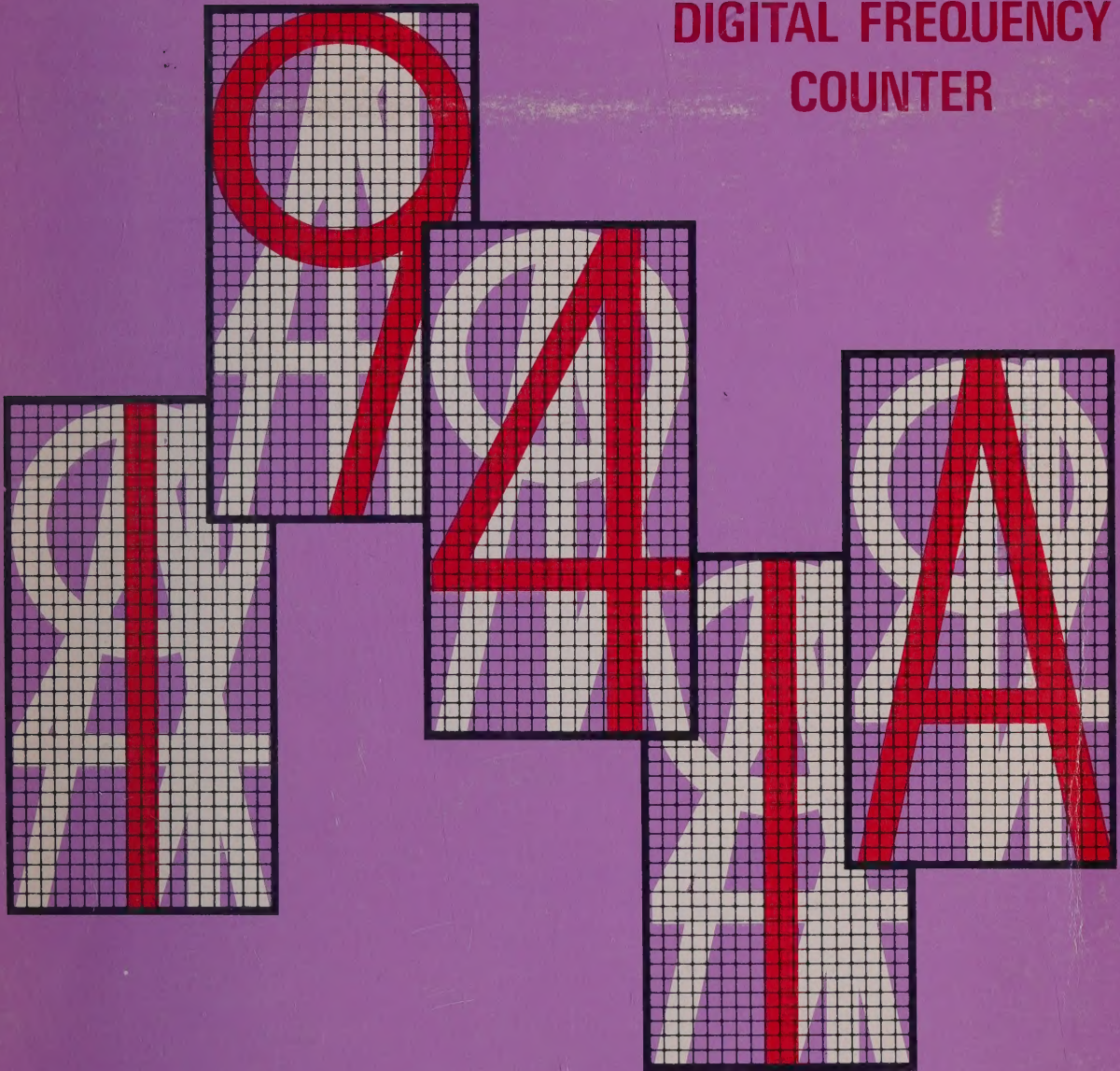
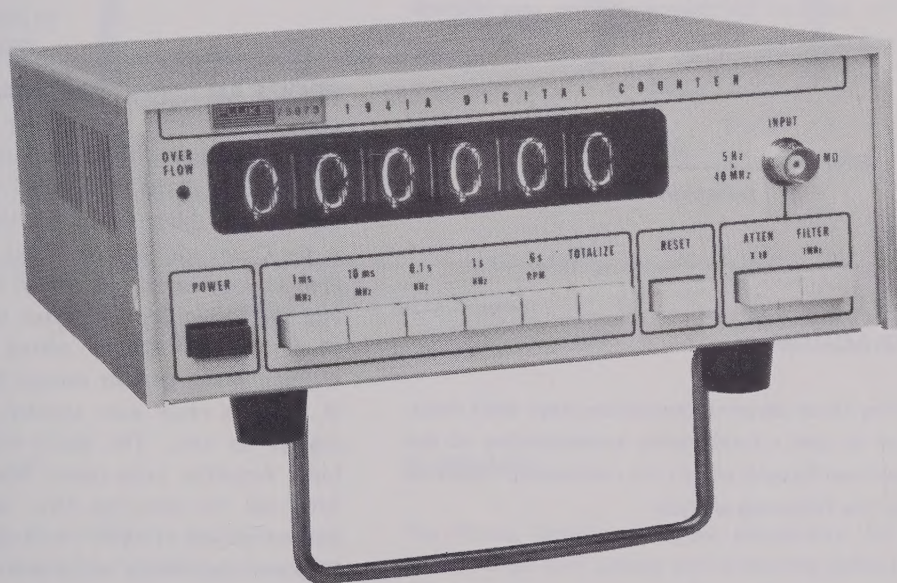


MODEL 1941A
DIGITAL FREQUENCY
COUNTER



Foreword

This training course has been prepared by the Customer Service Department of the John Fluke Mfg. Co., Inc. to assist the experienced technician to understand how the instrument works, how to calibrate it and how to maintain it. Should you have any questions, comments or suggestions about this course of instruction please feel free to communicate them to the Training Department by letter or telephone.



**CUSTOMER SERVICE TRAINING DEPT.
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INTRODUCTION

It is the purpose of this workbook to present the reader with enough information about the theory of operation and methods of repair to make it possible for a technician to efficiently maintain, calibrate, and repair the 1941A. This manual was intended to supplement the audio-visual training program on the 1941A Digital Counter.

The Model 1941A is a digital counter that will accurately measure inputs of 5 Hz to 40 MHz and display the count on a six digit neon display. There are two gating conditions for this instrument. One, manual, where the user selects gating periods at his discretion, the other is an internal gating condition which is selected by the gate time switches located on the front panel. When the RPM pushbutton is selected, the Model 1941A will display the speed of a one hundred pulse per revolution greater in RPM's. The formula for generators with output other than 100 pulses/rev is:

$$\text{RPM} = \frac{100}{\text{pulses/rev}} \times \text{display.}$$

BLOCK DIAGRAM

The following block diagram descriptions have been included in order to give a fundamental understanding of the various functional circuits within the instrument. Refer to Figure 1 for the following analysis.

POWER SUPPLIES

The power supply section of the 1941A generates three separate voltages that are utilized within this instrument. +170V is used to strobe on the display tubes, +5V for logic voltages, and a +10V which is used for operating voltage, through the instrument.

CLOCK

The Clock circuit generates a stable frequency of 10 MHz which is used for the timing of the instrument. This 10 MHz signal is first generated then converted to TTL logic, which is a square wave that pulses at a frequency of 10 MHz and

at a level of from 0V to a positive logic level voltage, typically +2V to +4V. The output of the Clock is then fed to a circuit called a Clock Divider.

CLOCK DIVIDER

The purpose of the Clock Divider is to so divide the Clock Output so as to produce one of two possible frequencies, dependent upon the Time selected on the front panel. This circuit is comprised of four groups of JK flip flops, three of which divide by 10, and one of which divide by 6. In all Time functions, except the .6s, the 10 MHz input to the Clock Divider is divided down to 10 kHz which is the Clock Divider output. In the .6 s (RPM) Function the Clock Divider output is 1.6666 kHz. The output of the Clock Divider circuit is fed to the Program Logic circuit.

PROGRAM LOGIC AND MAIN GATE

Since the action of these two circuits are interwoven they are analyzed at the same time. Note that there are two outputs from this circuit, one to the Main Gate, and another to the Count and Display Circuit. It is the function of the Program Logic circuit to convert the Clock Divider output into the timing Control Signals of this instrument. First of all the Clock Divider output is applied to a series of dividers, whose outputs control the Main Gate operation. If the 1ms range were selected, the Main Gate will be enabled for 1ms. This would allow any output from the Input Amplifier to be passed thru the Main Gate for 1ms. After the 1ms time the Main Gate will be disabled for another period of time. It is during this time that the Program Logic circuit will activate some circuits within the Count and Display section. This will be explained in the Schematic diagram analysis.

INPUT AMPLIFIER

The Input Amplifier will amplify the input signal, then shape the amplified signal into squarewaves. The squarewaves are then translated into pulses that pulse from 0V to a positive logic level (+5V). The frequency of the square-wave output is the same as the frequency of the input, and this output is applied to the Main Gate. It is this signal that is fed to the Count and Display circuit, when the Main Gate is enabled.

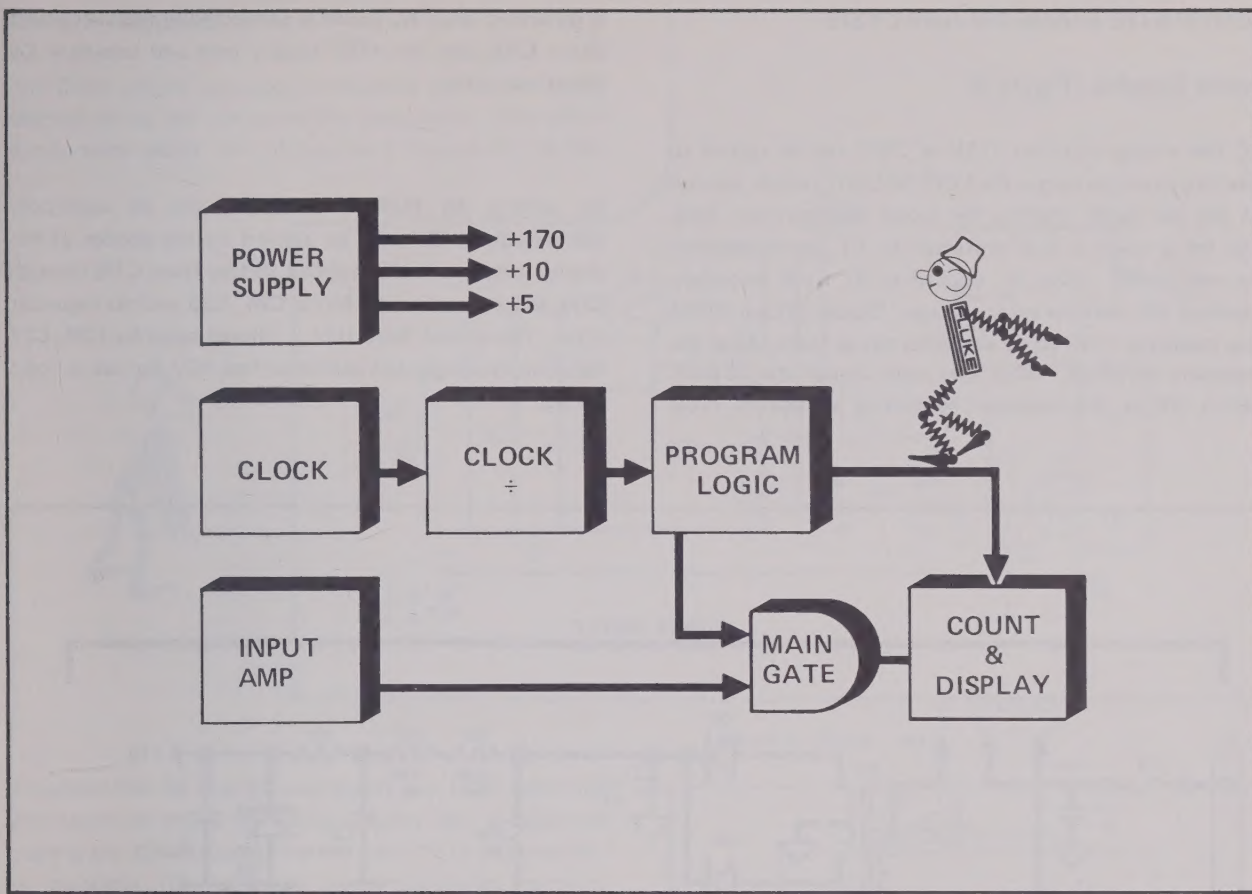


Figure 1. 1941A Block Diagram

COUNT AND DISPLAY

It is the purpose of the Count and Display circuit to count the pulses received from the Input Amplifier through the Main Gate, and display that count at the proper time. The Program Logic circuit controls the time for display and the time for resetting the counters to zero. If the count exceeds the display capability of the range selected, the Overflow indicator on the front panel will illuminate to show that condition.



SUMMARY

The Power Supply gives the instrument the operating voltage, logic level voltage and a strobing voltage when the instrument is turned on. This will cause the Clock to oscillate at a frequency of 10 MHz which is then divided down to a 10 kHz signal and applied to the Program Logic circuit. If the 1ms range is selected, the Program Logic circuit will enable the Main Gate for 1ms. The signal applied to the input of the 1941A will be amplified and converted to squarewave form and fed to the Main Gate. When the Main Gate is enabled the pulses out of the Input Amplifier will be fed to the Count and Display circuit. This will cause the BCD counters within this circuit to be serially loaded. The Program Logic circuit will then disable the Main Gate and cause the BCD count in the counters to be displayed, after which the counters are reset to zero and the Main Gate will again be enabled for 1ms. The display shows all digits at the same time and will continually display the latest input count.

SCHEMATIC DIAGRAM ANALYSIS

Power Supplies (Figure 2)

AC line voltage of either 115V or 230V can be applied to this instrument as long as the LINE SELECT switch, located on the rear panel, is set to the proper configuration. Note that the primary is fuse protected by F1, also located on the rear panel. With AC applied to J1, both secondary windings will develop an ac voltage. Diodes CR3 and CR4 plus capacitor C22 rectify and filter the ac from one of the secondary windings. Note that even though the POWER switch, S2, is not depressed, operating voltage of +10V

is generated when AC power is connected to the instrument. Zener CR5 sets the +10V supply level and capacitor C6 filters out noise.

By setting the POWER switch to the on condition, (depressed), +170V will be applied to the anodes of the display tubes, and the rectified voltage from CR6 through CR9 will be applied to filters C24, C25 and to regulator U14. The output from U14 is filtered again by C26, C27 resulting in a regulated and noise free +5V for use as logic voltage.

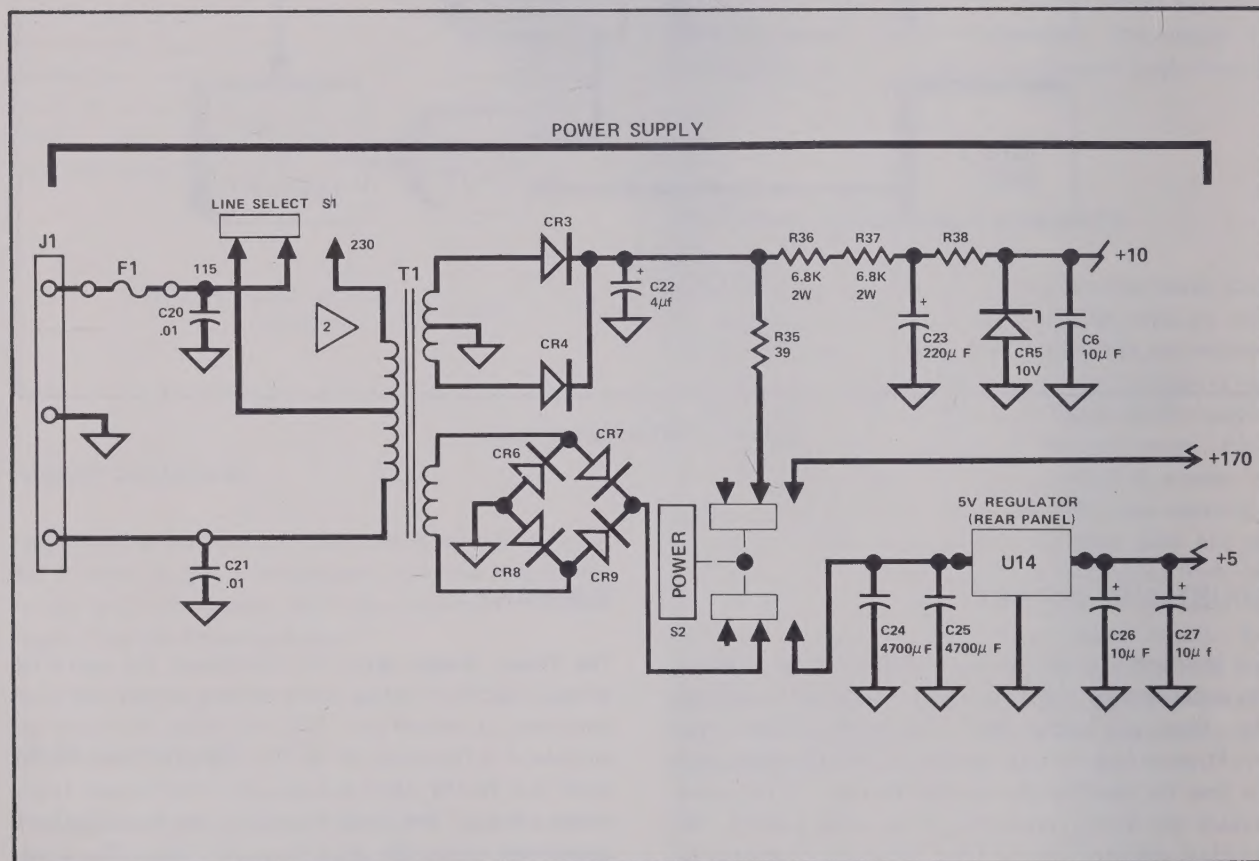


Figure 2. Power Supply

CLOCK (Figure 3)

The Clock circuit generates a frequency of 10MHz that is utilized to set the timing of this instrument. The active components within this circuit are a Crystal Y1, Buffer

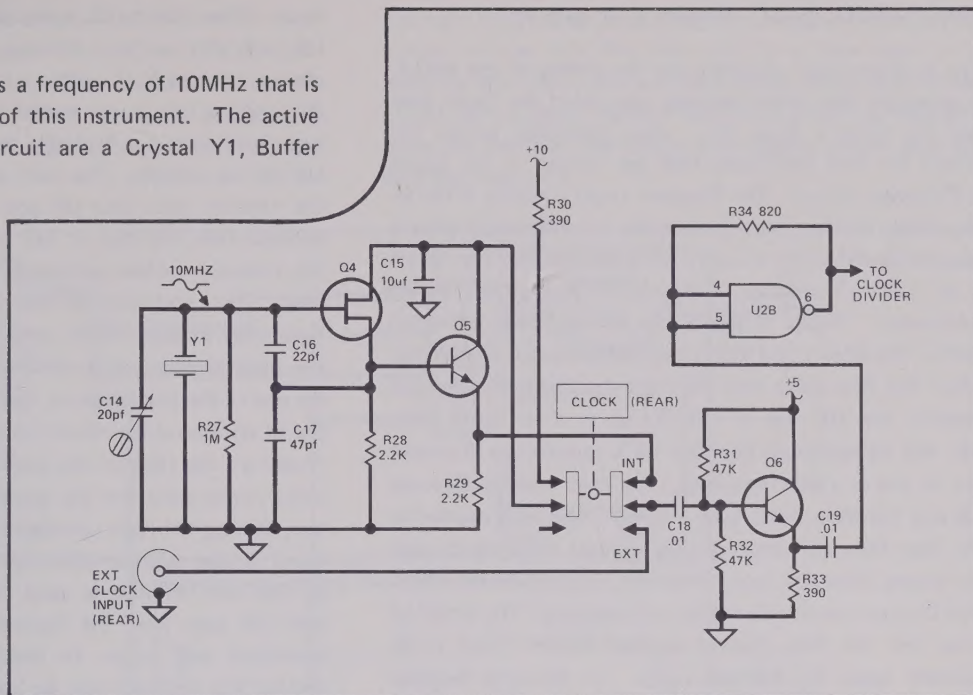


Figure 3. Clock

Amplifier Q4, Q5 and Q7 and NAND gate U2B. With the application of +10V, the clock circuitry will be activated causing the 10 Mhz signal from crystal Y1 to be amplified by transistor Q5. Q4 acts as an impedance matching device to eliminate possible loading of the crystal, and C14 is used to adjust the 10 MHz signal during final calibration. The output of Q5 is then fed across the clock switch, in the INT position, to the base of Q6. Q6, with its associated circuitry, is another buffer amplifier which is used for impedance matching between its input and the input to NAND gate U2B. The impedance matching of Q6 is mainly for use with an external clock input, although it is always in the signal path to the input of U2B. U2B will translate the output of Q6 into a TTL format and consequently drive the Clock Divider.

CLOCK DIVIDER (Figure 4)

The Clock Divider is comprised of three series connected divide by 10 dividers, (U4, U5 and U6) followed by a divide by 6 divider, (U6). The input to this circuit is the 10 MHz TTL signal output of U2B. The output in all range positions except the .6s range, is the QD output line from the last divide by 10 divider U6. This output, a 10 kHz signal, is then fed to the Program Logic section. Divider U7 is utilized in the .6s range only, at which time the output of the clock divider will be 1.666 kHz.

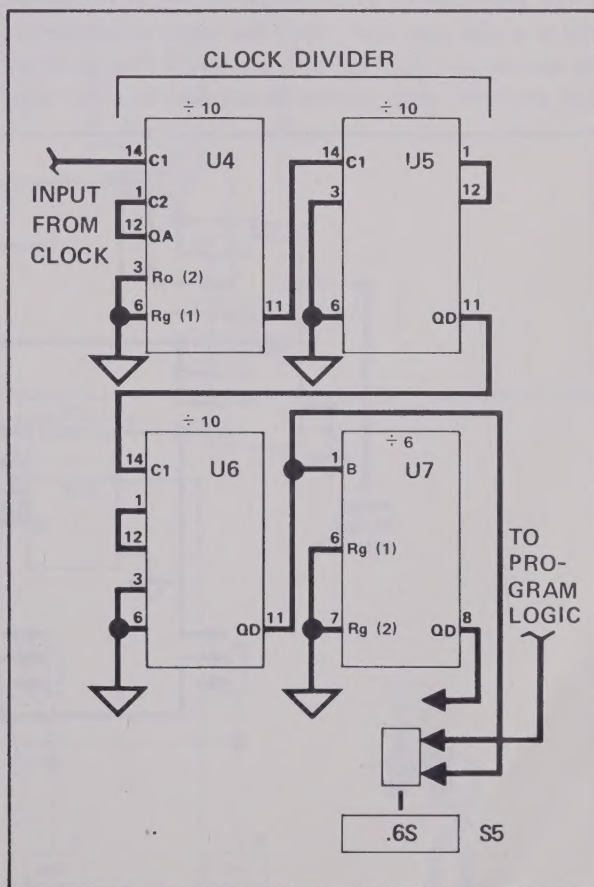
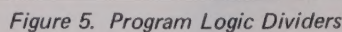


Figure 4. Clock Divider

The program Logic circuitry sets the timing of the 1941A. It generates two timing periods, one called the Count time and the other a Time Out. Also generated within this circuit are two commands that are utilized in the Count and Display circuit. The Program Logic circuitry is fed by the Clock Divider output. In order to understand what is happening within this circuitry let us assume that the 1941A is set to the 1ms range. Figure 5 and 6 are the program schematics. Figure 7 shows the timing pulses generated within this circuit and their relationship toward each other. When the first pulse into U9 from the Clock Divider goes negative the QD line of U9 will go to a low logic level, this will be fed to JK flip flop U13, causing the Q output line to rise to a high logic level. This level is fed to Decoder U8 and the Main Gate, U2A. A high logic level applied to the Main Gate will cause it to be enabled, allowing the output pulses from the Input Amplifier to be fed to the Count and Display circuit where they are counted. The length of time that the Main Gate is enabled (Count Time) is dependant upon the selected range. In this case the 1ms range has been selected, therefore the Main Gate will be enabled for 1ms. Since the high level output of U13 is fed to U8, Input line D, all of the output lines of U8 will be held at a high logic level. When the eighth pulse input to U9 will rise to a high logic level and stay in that condition until the tenth pulse applied to U9 goes to a low logic



A high level out of U3B will cause the dividers U9 through U12 to go to a low level, which will set the Q output of the first flip flop U13 to a high logic level, enabling the Main Gate and setting the instrument in the Count period again. NAND Gate U2D is used to manually reset the Dividers, the Count and Display circuit plus the first flip flop U13.

through U12 to go to a low level, which will set the Q output of the first flip flop U13 to a high logic level, enabling the Main Gate and setting the instrument in the Count period again. NAND Gate U2D is used to manually reset the Dividers, the Count and Display circuit plus the first flip flop U13.

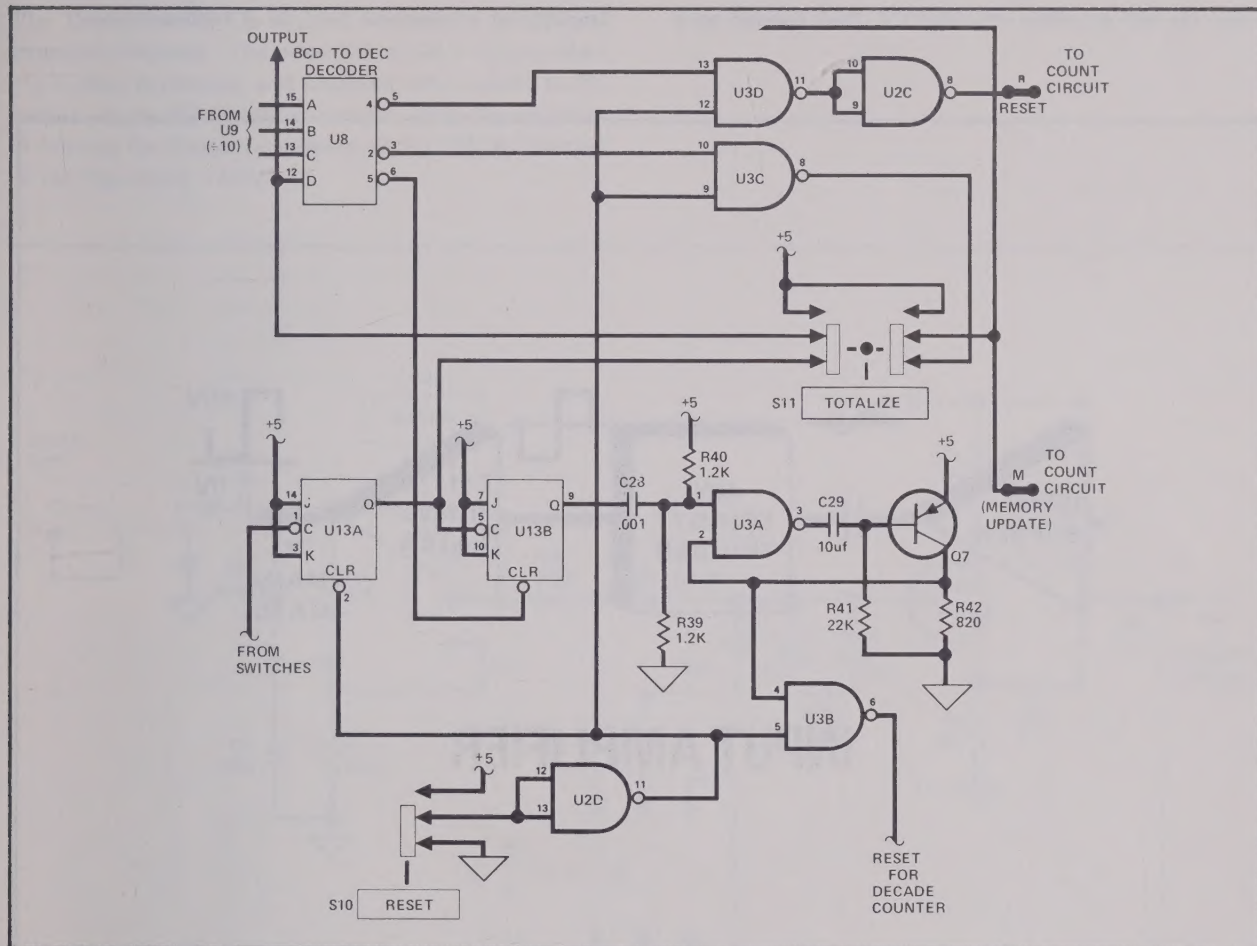


Figure 6. Program Logic

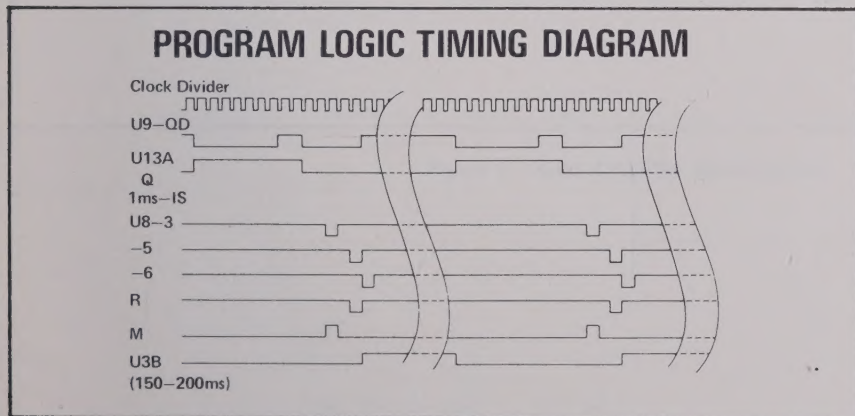


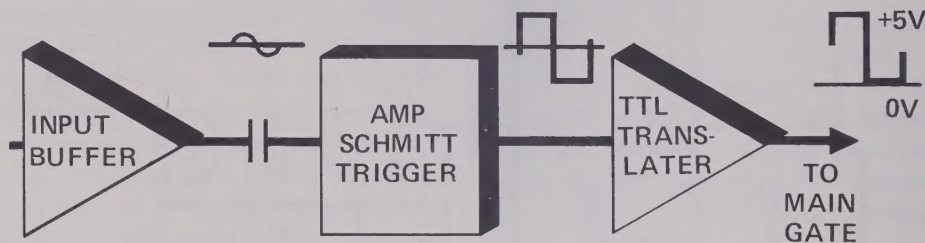
Figure 7. Timing Diagram



INPUT AMPLIFIER (Figure 8)

Looking at Figure 8, Block Diagram of the Input Amplifier, we can observe what happens to the Input signal. The input signal is first applied to an attenuator network of either X1 or X10. The input is then taken off the attenuator and applied through filtering into the AC Amplifier. From the AC Amplifier the signal is then applied to a

Schmitt Trigger which is utilized to generate a square-wave signal from the input signal. This squarewave signal is then applied to a TTL converter which converts the squarewave into TTL format, which is then fed to the Main Gate, U2A. The purpose of the Input Amplifier is to condition the input signal into a format that can be utilized in the Count and Display circuit. Analysis of the Input Amplifier at a schematic level, is as follows.



INPUT AMPLIFIER

Figure 8. Input Amplifier Block Diagram

Attenuator and Filter

The input signal is applied across capacitor C1 to the Attenuator network of R1, R2 and capacitors C2, C3. Switch S3, located on the front panel of the 1941A, is used to select the amount of attenuation desired. In the X10 position, the input signal is attenuated by a factor of 10. Capacitors C1, C2, C3, and C4 give the 1941A its frequency response. The placement of C4 is altered when FILTERing is selected, and Capacitor C5 is added to the output of the AC Amplifier circuit. With the selection of filtering the frequency response of the 1941A is limited on the high end to 1 MHz.

AC Amplifier (Figure 9)

Diodes CR1 and CR2 on the input to the AC Amplifier form a protection circuit that will limit the input voltage to the amplifier in cases of overloading. The AC Amplifier circuit is comprised of Q1, Q2 and associated circuitry, with Q1 acting as a buffer amplifier. The output of this amplifier is fed through C7 to the input of a Schmitt Trigger.

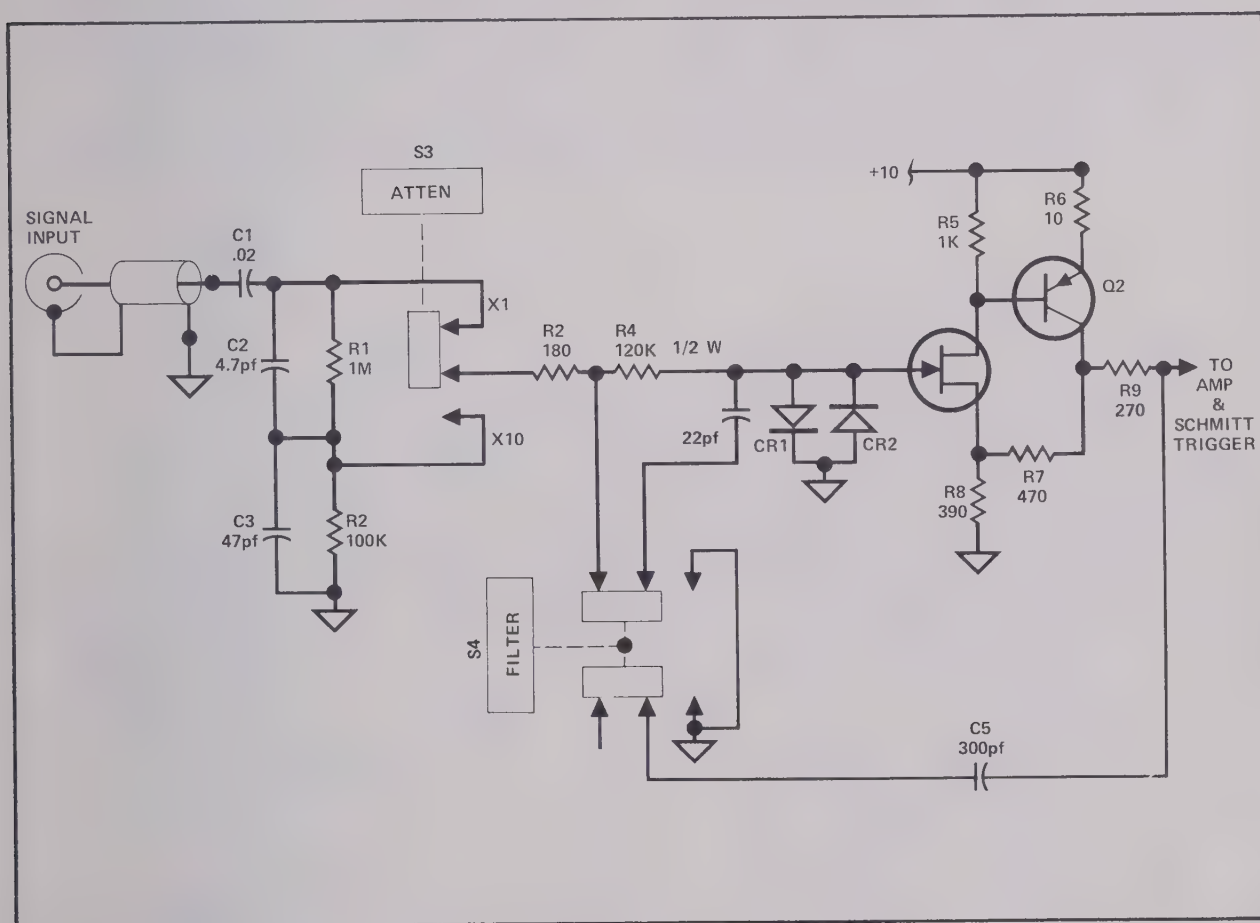


Figure 9. Input Amplifier Input Section

Schmitt Trigger (Figure 10)

This circuit is comprised of U1A, U1B and U1C. The input to this circuit comes from the AC Amplifier output into pin 9 of U1A, pin 9 being the +input terminal. Pin 10 is - input terminal and note that it is connected to an adjustment labeled TRIG LEVEL PRESET. This adjustable resistor, R10, sets the operating level of the Schmitt Trigger by setting the level on the input to U1A. When the input on pin 9 reaches the preset level of pin 10, U1A will operate, thus placing signals on it's output terminals pins 6 and 7. Pin 6 will carry the positive going signal while pin 7 will carry the negative going signal. Both of these signals will be equal in amplitude but opposite in polarity. The outputs of U1A are then coupled to the inputs of U1B, pin 4 being the positive input and pin 5 the negative input. Due to the gain of U1B when it's input signals deviate

from their reference point, both outputs will quickly rise or fall. This will result in a squarewave output on both output legs. Here again the amplitude of the signals on both output legs are the same, but when the positive output terminal is high the negative output terminal is low and the inverse is also true. The squarewave outputs from U1B are then applied to U1C, which is used for isolation purposes so that the Schmitt trigger circuitry is not loaded by succeeding circuits. Transistor Q3 is used as TTL Converter in order to convert the squarewave outputs of U1C into TTL format. The base and emitter of this transistor are connected to the outputs of U1C, and the collector, the output of the Input Amplifier, is connected to the Main Gate. The squarewave signal on the output of the Input Amplifier will fluctuate from 0 to approximately 5V. The frequency of this signal is the same as the input signal.

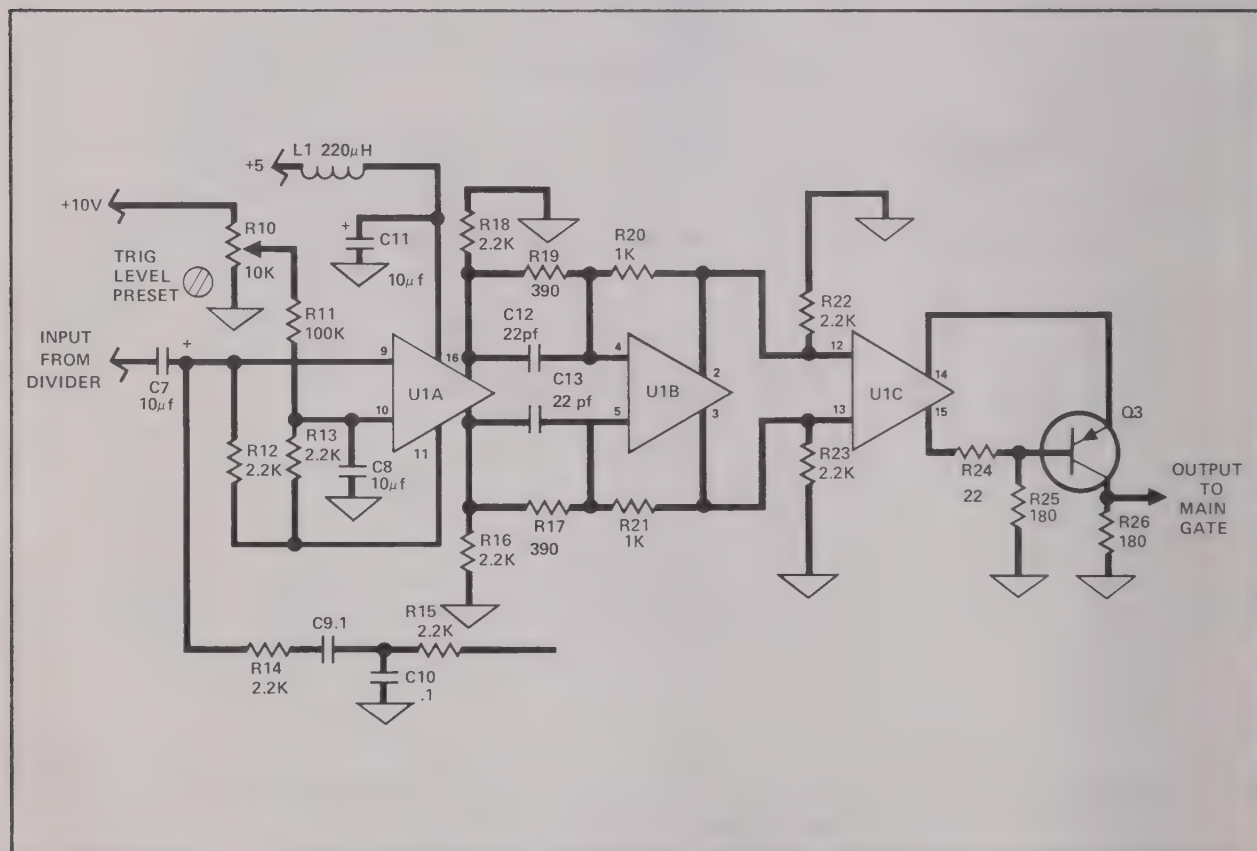


Figure 10. Input Amplifier Schmitt Trigger



COUNT AND DISPLAY (Figure 11)

This circuit is comprised of six BCD counters, six Quad Latches, six Decoder Drivers, and six display tubes. Analysis of this circuit will be accomplished by analyzing one section comprised of a BCD Counter, Quad Latch, Decoder Driver, and Display tube, as all six digits are processed exactly the same. Once the Main Gate is enabled, the pulses from the Input Amplifier are applied to the BCD Counters, which are serially loaded, and convert the pulses into a BCD format. The BCD Counters will continue to count the input pulses and convert the count into a BCD format until the Main Gate is disabled by the Program Logic circuit. After the Main Gate is disabled the Count circuit will receive from the Program Logic circuit a Memory Update (M) command into the Quad Latch. This will enable the Quad Latch, passing the BCD count of the BCD Counter on to the Decoder Driver. The Decoder Driver will convert the BCD count into a decimal format by driving to a low (0V) potential the proper decimal line on it's output. This will

place a low potential on the display tube which already has a +170V on it's anode, thus a number will be displayed on the tube. The Quad Latch is then disabled and the BCD Counter is cleared by the Reset command (R) from the Program Logic circuit. This conditions the count circuit to be ready to count when the Main Gate is again enabled. The display will remain constant until the next input has been counted by the BCD counter and the (M) command closes the Quad Latch. U33A and U34A through U34D, pulse the Overflow LED constitute an overrange indicator. If the BCD Counters are fully loaded and another pulse is received through the Main Gate from the Input Amplifier, the last BCD Counter, U30, will set U33A so it's output (Q) will go high (+5V), thus placing a high potential on one input of NAND Gates U34A and D. This sets the Overflow circuitry. When the Memory Update (M) command is applied to the Count circuit it will place a high potential to the second input to U34A, causing a low potential to be applied to one side of the Overflow Indicator, thereby illuminating it.

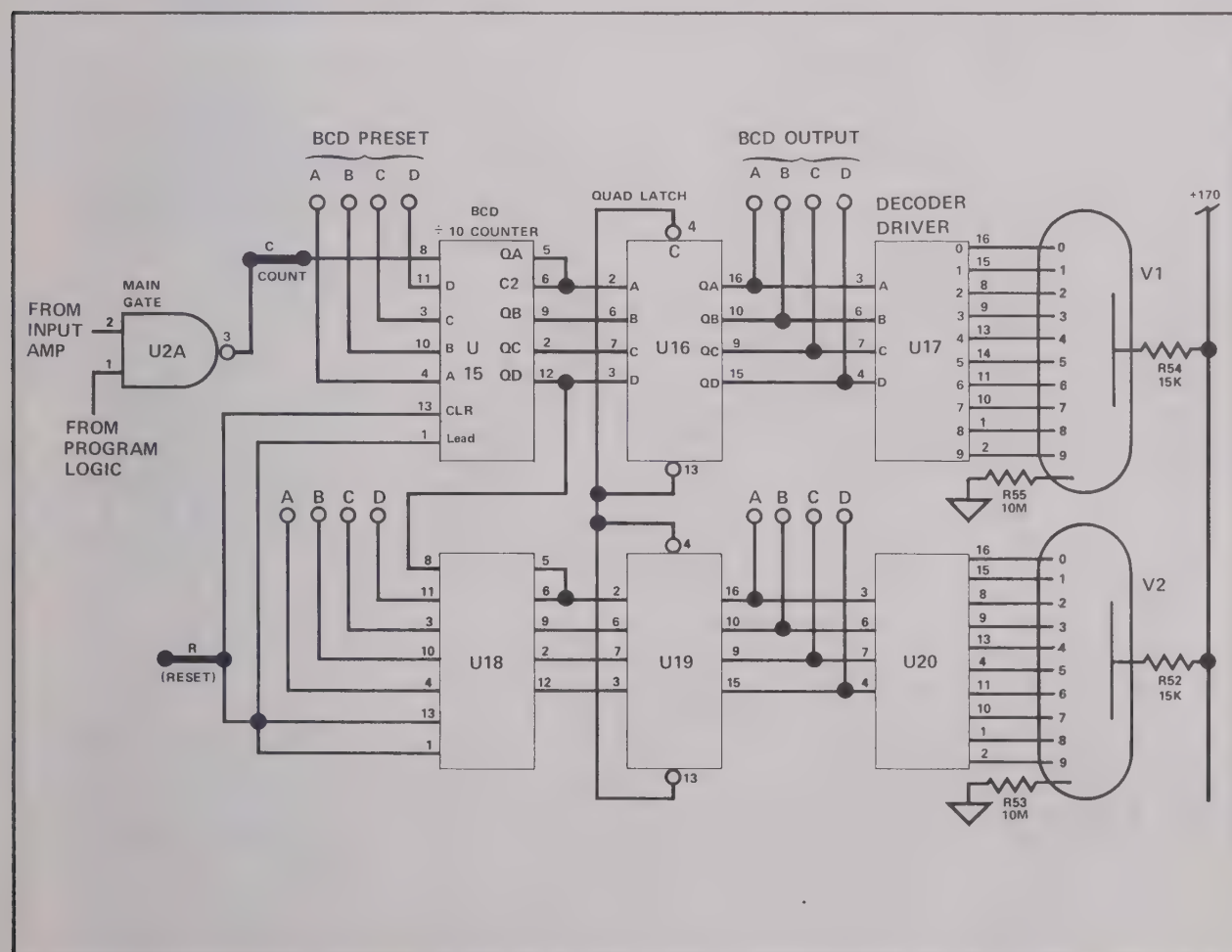


Figure 11. Main Gate, Count & Display

TROUBLESHOOTING

Effective troubleshooting of the 1941A starts with observing indications of trouble on the display. By manipulating the front panel controls for different conditions, some circuitry can possibly be discounted as a source of the problem. To efficiently use this technique a technician needs to know the theory behind this instrument.

This section of the 1941A Student Handout contains a Troubleshooting Flow Chart, idealized waveforms, and hints on how to best troubleshoot this instrument. By following the Troubleshooting Flow Chart (Figure 12) troubles can be isolated to specific sections of the instrument (i.e., Input Amplifier, Clock, Program Logic, Count and Display circuits).

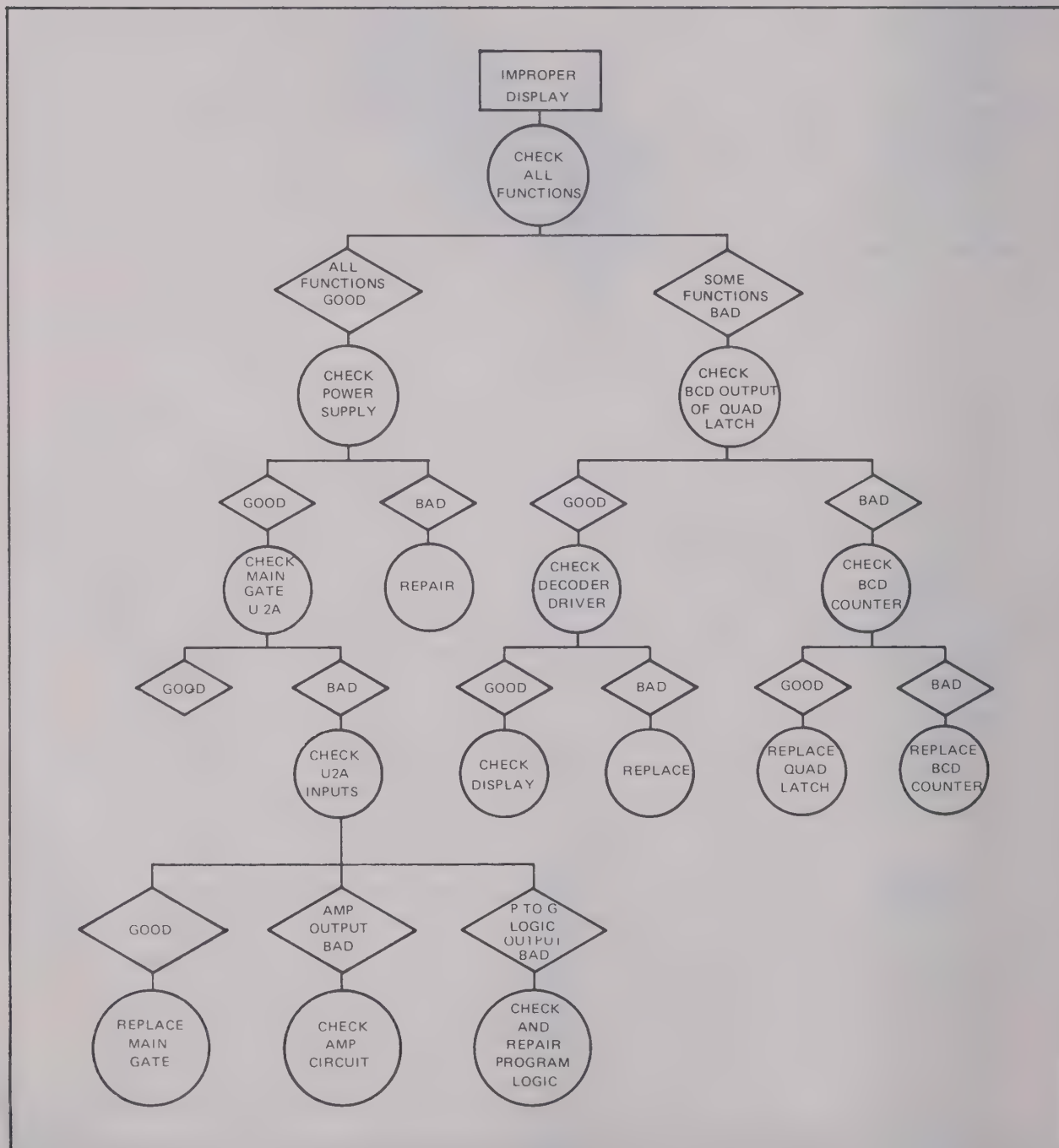


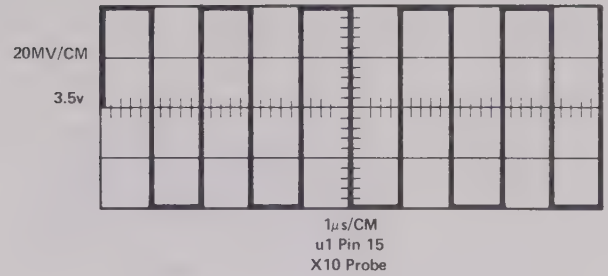
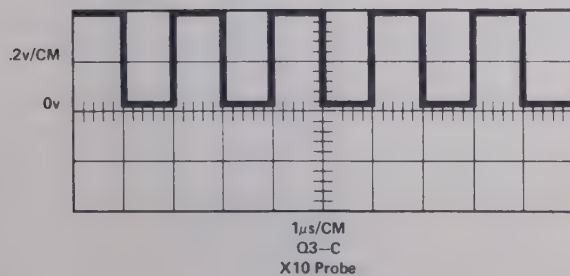
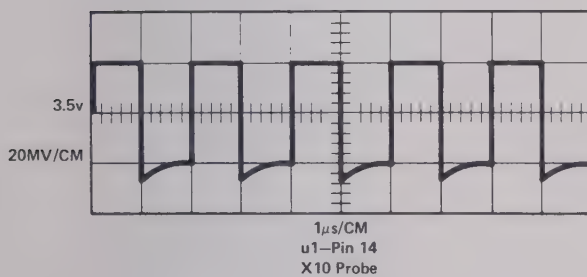
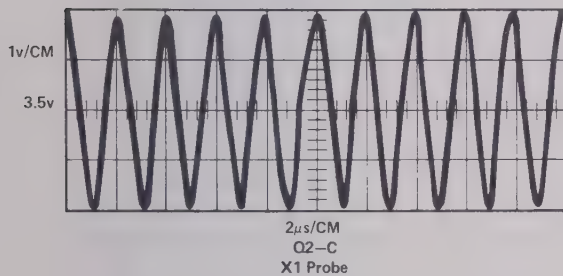
Figure 12. Troubleshooting Flow Chart

The following idealized waveforms were taken from an instrument and accurately redrawn for use in this Student Handout. The condition of the 1941A for these waveforms is as follows:

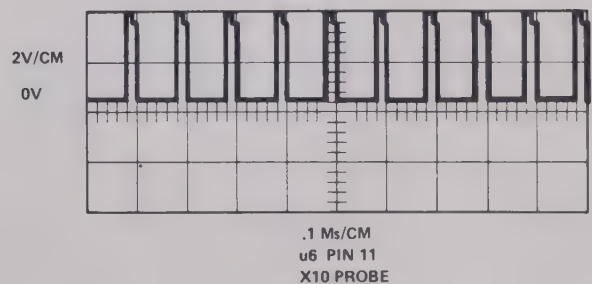
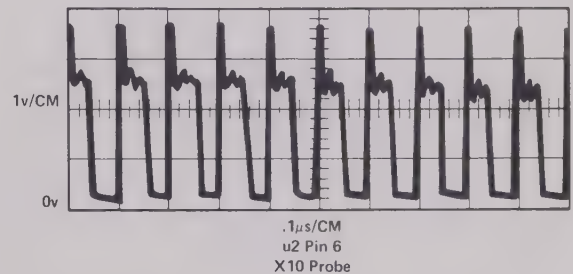
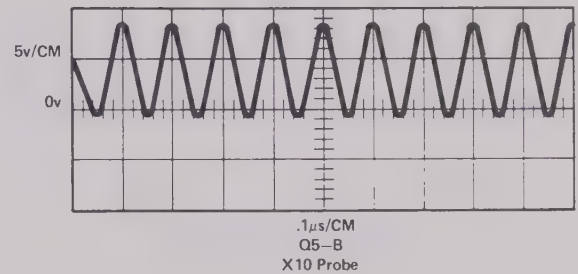
Range .1s
 ATTN X1 (Switch in the non-depressed position)
 FILTER OUT (Switch in the non-depressed position)
 INPUT 500 kHz, 40 Mv

The scope that was used to check these waveforms was a Tektronic Model 485. Note that below each waveform is the information as to where the waveform can be found, the scope probe that was utilized to get that specific waveform, and the scope settings. A + Trigger level was utilized on the 485 scope.

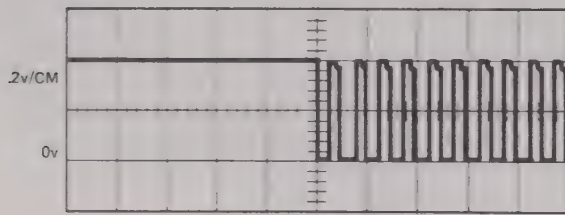
INPUT AMPLIFIER



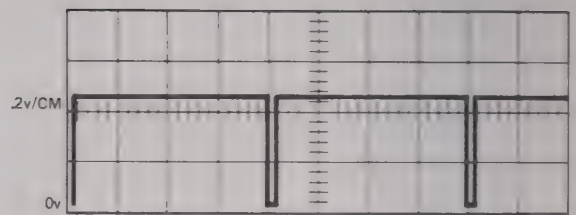
CLOCK AND CLOCK DIVIDER



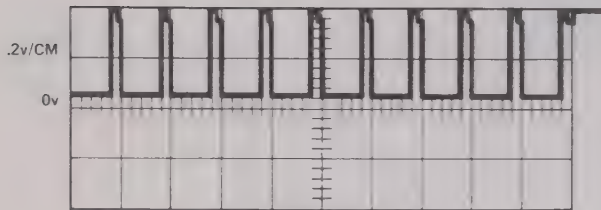
PROGRAM LOGIC



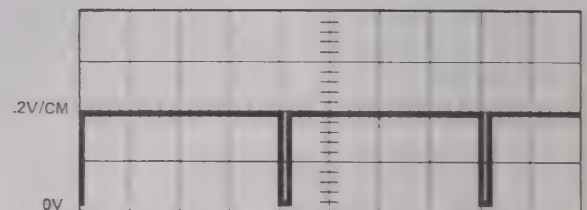
20MS/CM
u10 Pin 11 (Ext Trig u12 Pin 11)
X10 Probe



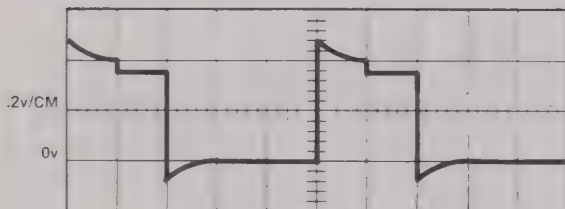
50MS/CM
u8 Pin 5
X10 Probe



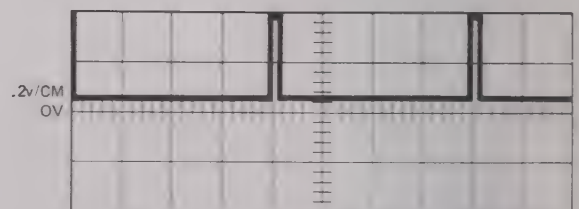
10MS/CM
u10 Pin 11 (Ext Trig u12 Pin 11)
X10 Probe



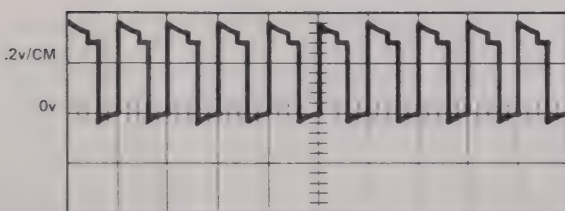
50 Ms/CM
RESET @ R
X10 PROBE



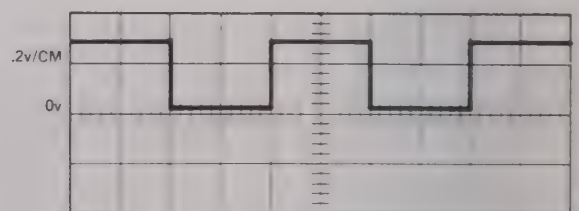
.2MS/CM
u8-Pin 13
X10



50MS/CM
Memory Update @ M
X10 Probe

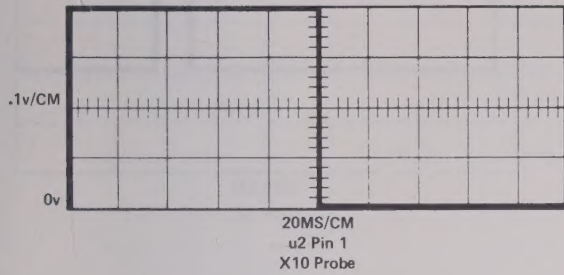


.2MS/CM
u8-Pin 15
X10
Pulsed @ Gate Time



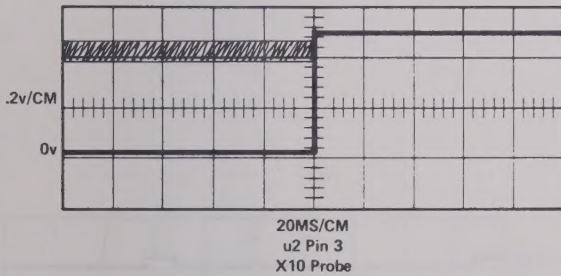
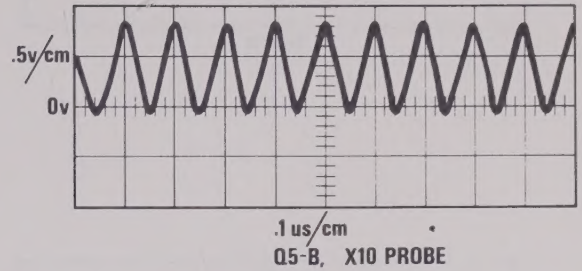
50MS/CM
u3 Pin 3 & 6 (5HI)
u12-Pin 11
X10 Probe

MAIN GATE

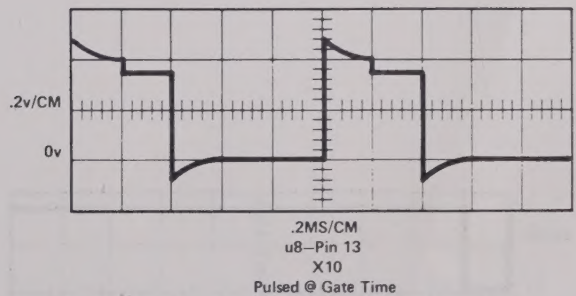
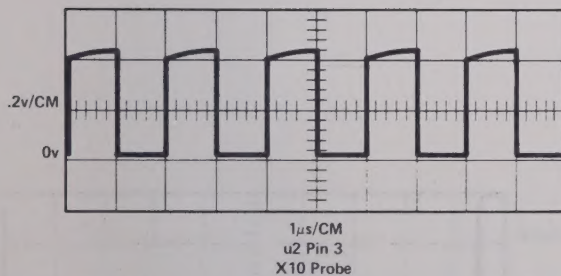
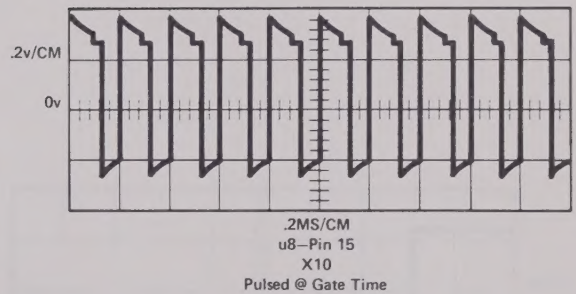


The following wave forms were taken with the same equipment but the gate time (range) of the 1941A was changed from $-1s$ to $10ms$.

CLOCK



PROGRAM LOGIC



PROGRAM LOGIC

